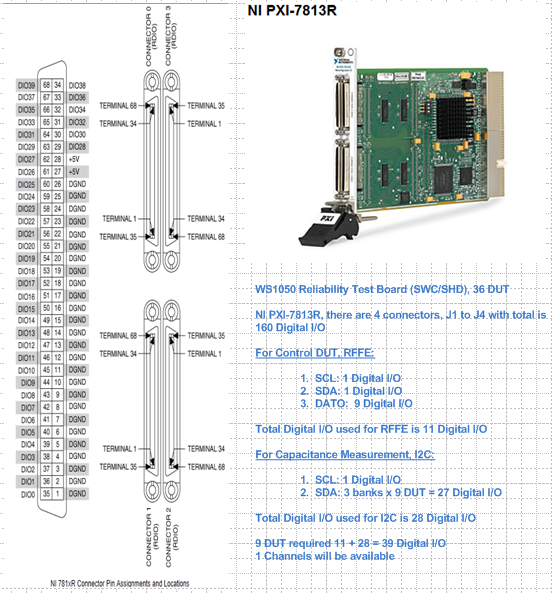
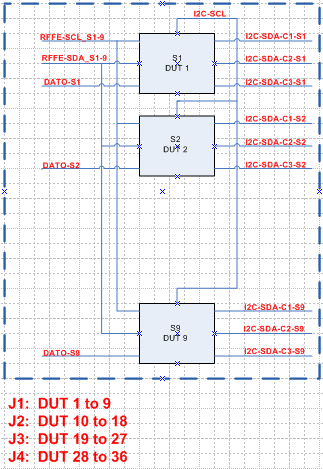
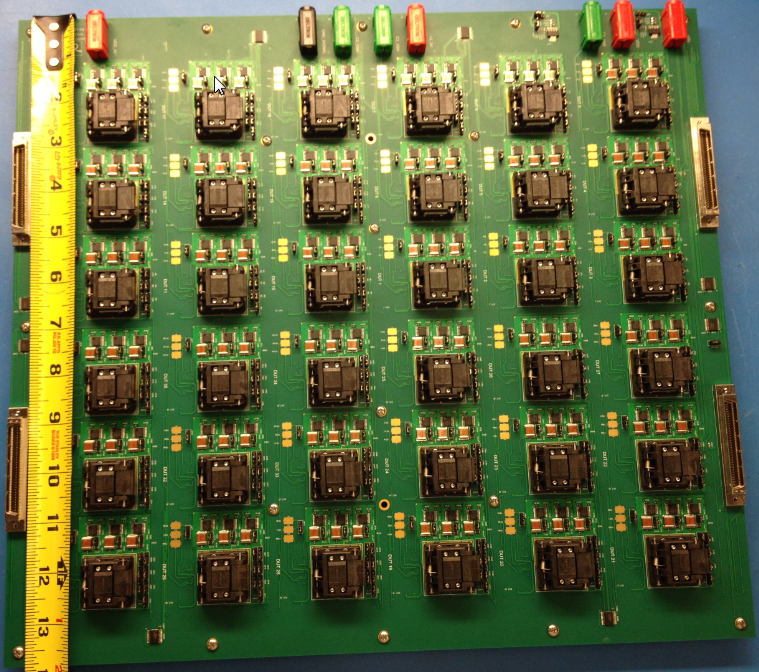
Design WS1050 Reliability Digital I/O

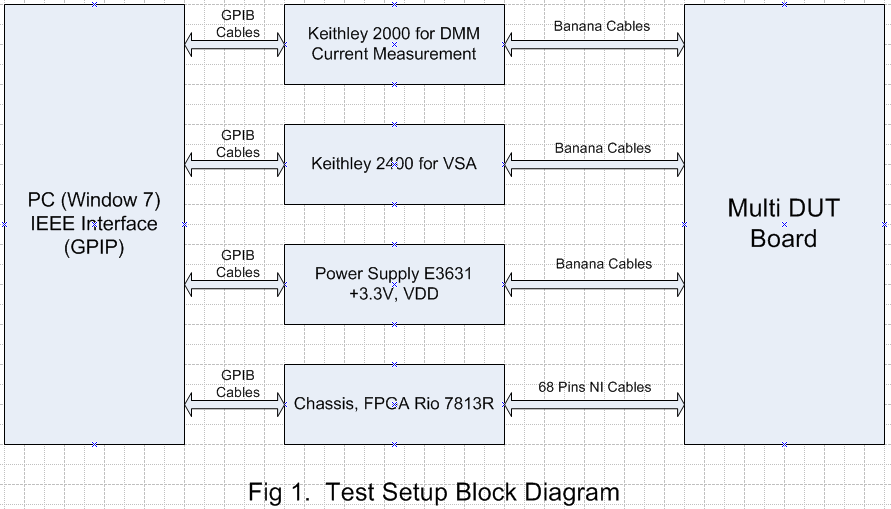
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**36 DUT Board Layout:**



Test Setup Block Diagram:



Hardware:

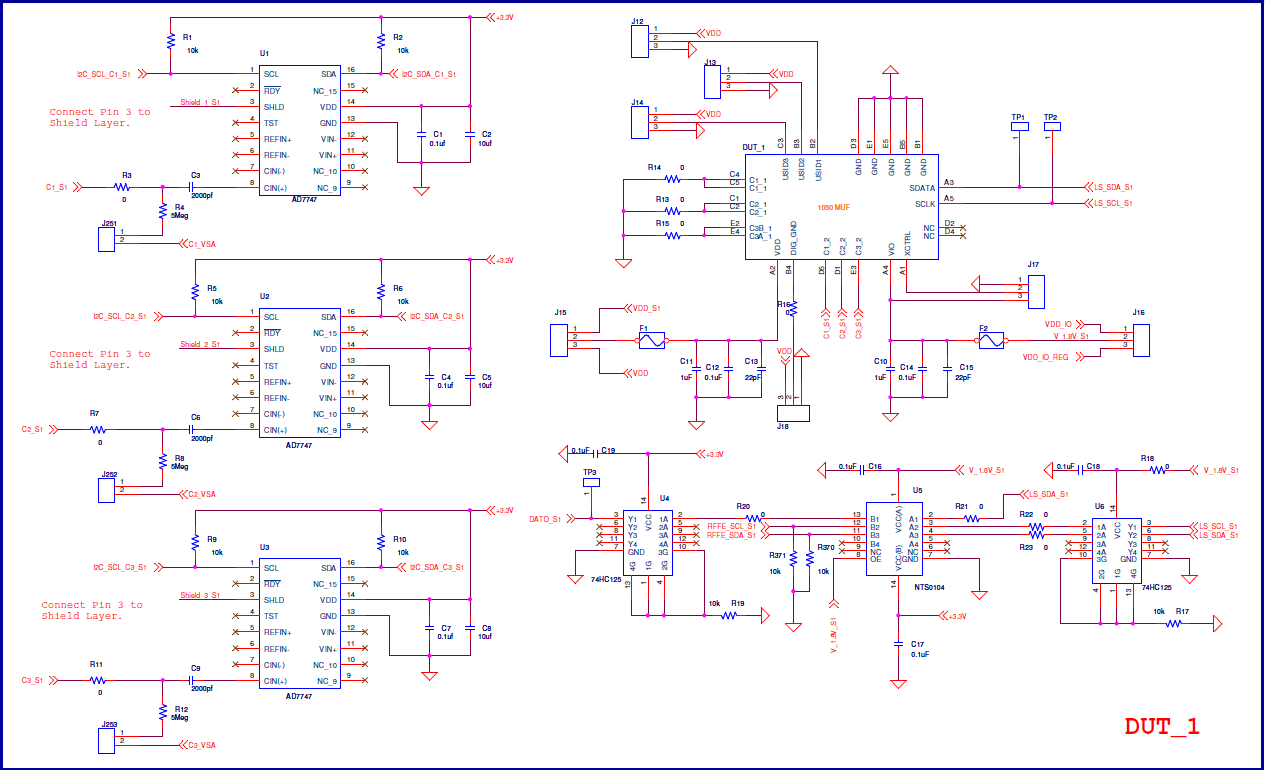
1. Keithley 2000 (DMM)
2. Keithley 2400 (Source meter for VSA test)
3. Agilent Power supply E3631 (Power source for +3.3V, VDD)
4. Chassis PXI 1033
5. FPGA card Rio 7813R, 160 digital I/O channels
6. SHC68-68-RDIO Cables (4)
7. Several banana plugs

Software:

1. FPGA Revision :
2. WS\_VCAP Driver 029 (36 DUT)
3. WS\_VCAP Driver 024 (16 DUT)
4. Stress Test Program
5. WS1050 36 DUT Reliability HD\_Cycling Ver1.3 (36 DUT)
6. WS1050 16 DUT Reliability HD\_Cycling Ver1.8 (16 DUT)

Schematic:

1. Schematic WS1050 36 DUT Reliability REV E.
2. Schematic WS1050 16 DUT Reliability REV G.



Test Sequences:

1. Turn ON +3.3V, this will turn on AD7747 and voltage regulator LM317 to generate 1.8V for VIO
2. Turn ON VDD (HD = 3.3V; Cycle = 3.7V)
3. Set CP OFF
4. Measure IDD standby
5. Set CP Voltage to stress
6. Set DVA (ON/OFF)
7. Set ECAL (ON/OFF)
8. Set VPI (ON/OFF) Note: If VPI OFF, skip steps 31 to 41.
9. Set VSA (ON/OFF) Note: If VSA OFF, skip steps 42 to 54.
10. Set HS (ON/OFF) Note: If HS check OFF, skip step 55.
11. Start HD/Cycle (Non linear RP).
12. Turn All Drivers ON
13. Measure IDD All Drivers ON
14. Turn All Drivers OFF
15. Measure IDD All Drivers OFF
16. Measure C1\_Min
17. Measure C1\_F1
18. Measure C1\_F2
19. Measure C1\_S1 to C1\_S14F12
20. Measure C1\_Min2
21. Measure C2\_Min
22. Measure C2\_F1
23. Measure C2\_F2
24. Measure C2\_S1 to C2\_S14F12
25. Measure C2\_Min2
26. Measure C3\_Min
27. Measure C3\_F1
28. Measure C3\_F2
29. Measure C3\_S1 to C3\_S14F12
30. Measure C3\_Min2
31. Set DVA OFF, ECAL OFF (this is for VPI)
32. Set CP Voltage for VPI
33. Measure C1\_Min
34. Measure C1\_Max
35. Measure C1\_Min2
36. Measure C2\_Min
37. Measure C2\_Max
38. Measure C2\_Min2
39. Measure C3\_Min
40. Measure C3\_Max
41. Measure C3\_Min2
42. Set Ke2400 to V1 = -10V
43. Measure VSA C1\_V1
44. Measure VSA C2\_V1
45. Measure VSA C3\_V1
46. Set Ke2400 to V2 = 0V
47. Measure VSA C1\_V2
48. Measure VSA C2\_V2
49. Measure VSA C3\_V2
50. Set Ke2400 to V3 = 10V
51. Measure VSA C1\_V3
52. Measure VSA C2\_V3
53. Measure VSA C3\_V3
54. Set Ke2400 to 0V.
55. Run HS check on Register 1 (bank C1)
56. Save Data
57. Loop back to step 11

Note:

Test Sequence: Test program can measure read point by bank order, C1-C2-C3; C2-C1-C3 or C3-C2-C1

Stress Sequence: Test program can stress parts by bank order by setting commands:

070201|XX|XX|XX

070201|XX|XX|XX

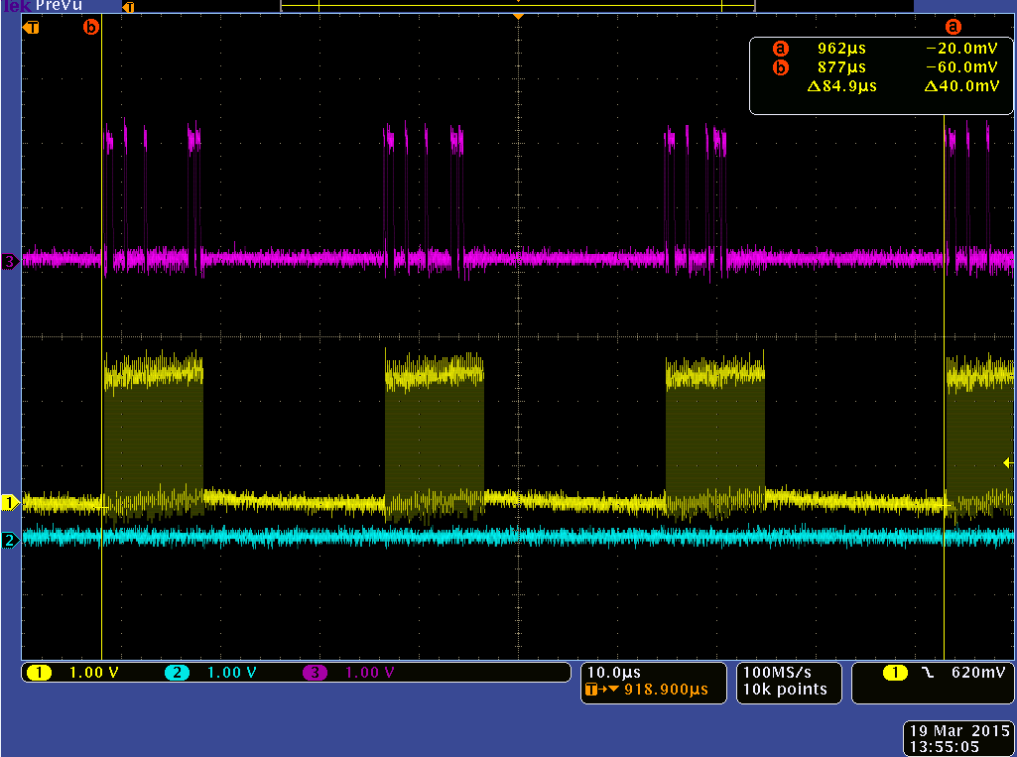
070201|XX|XX|XX

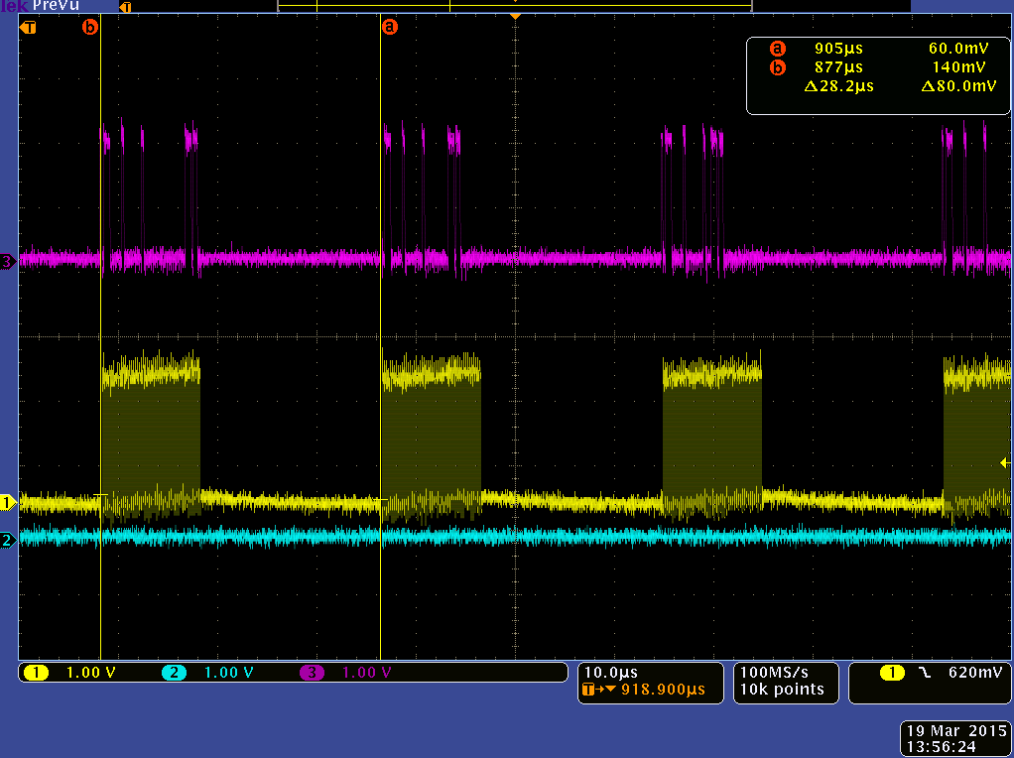
XX can be 3B all drivers ON

XX can be 00 all drivers OFF

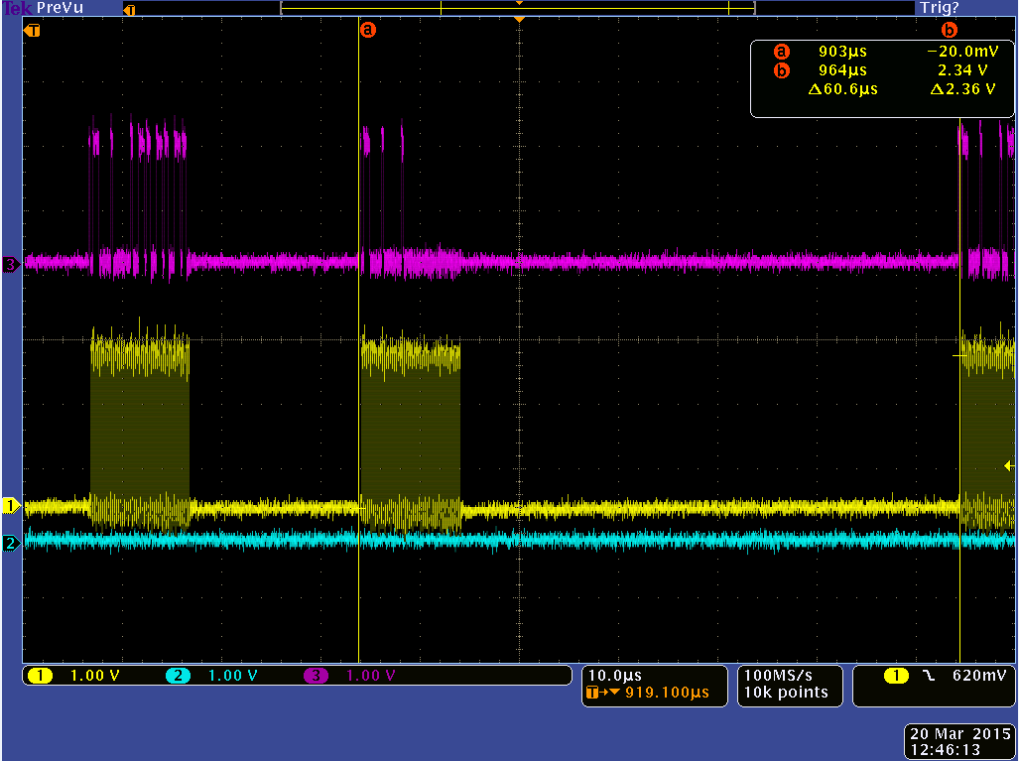
Cycling speed is12KHz with signal CLK is 5MHz.

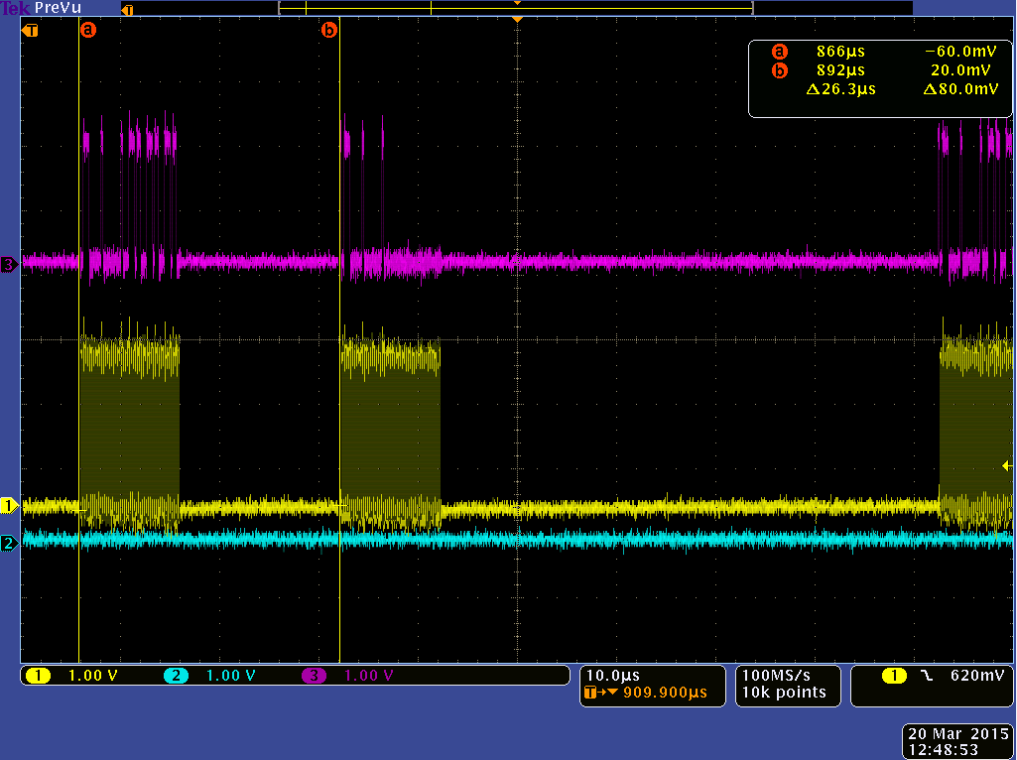
With 33% Duty Cycle:



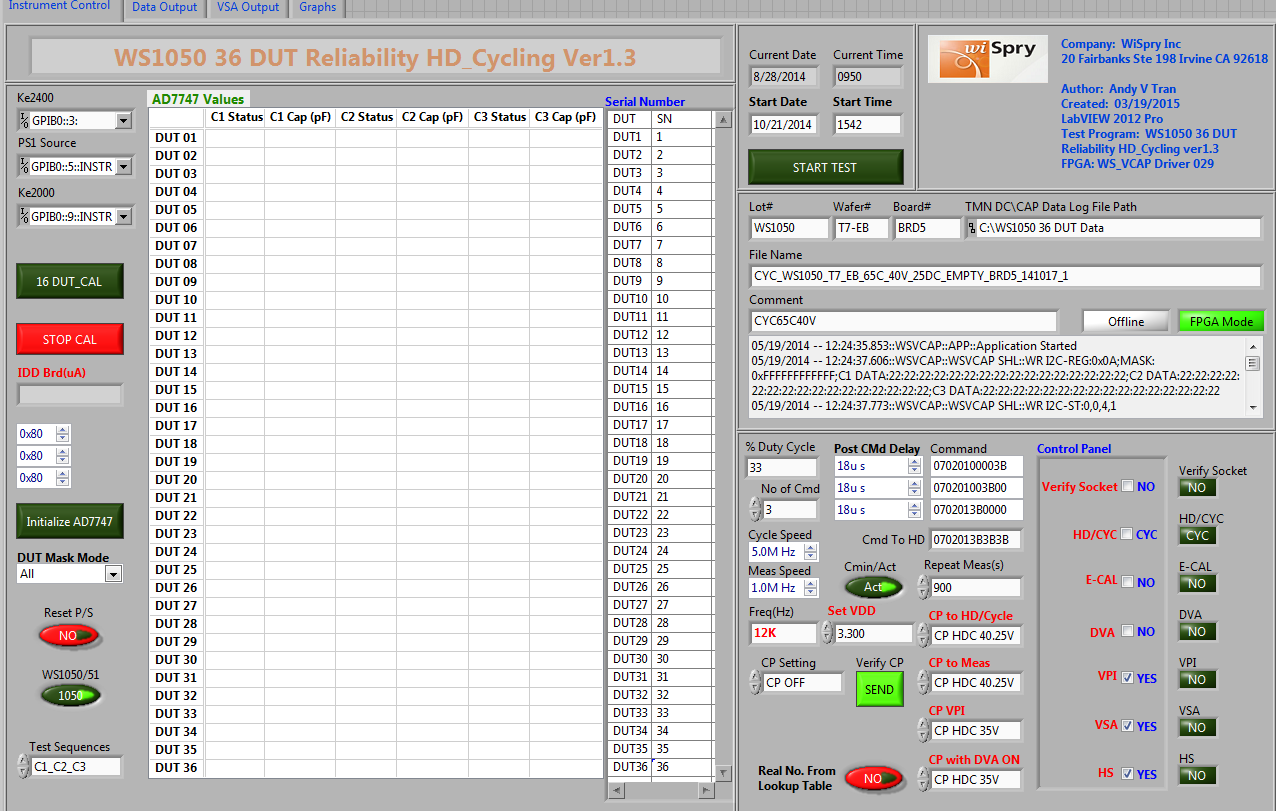


With 25% Duty Cycle

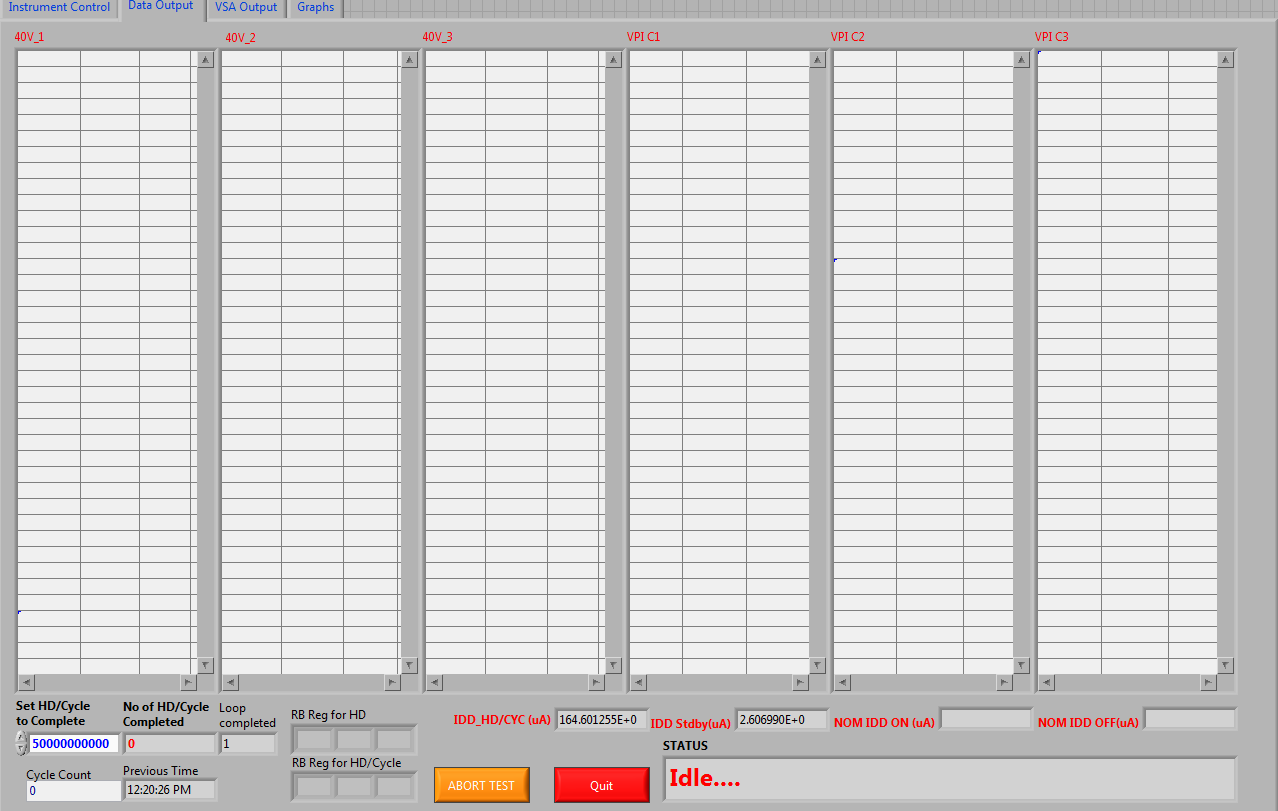




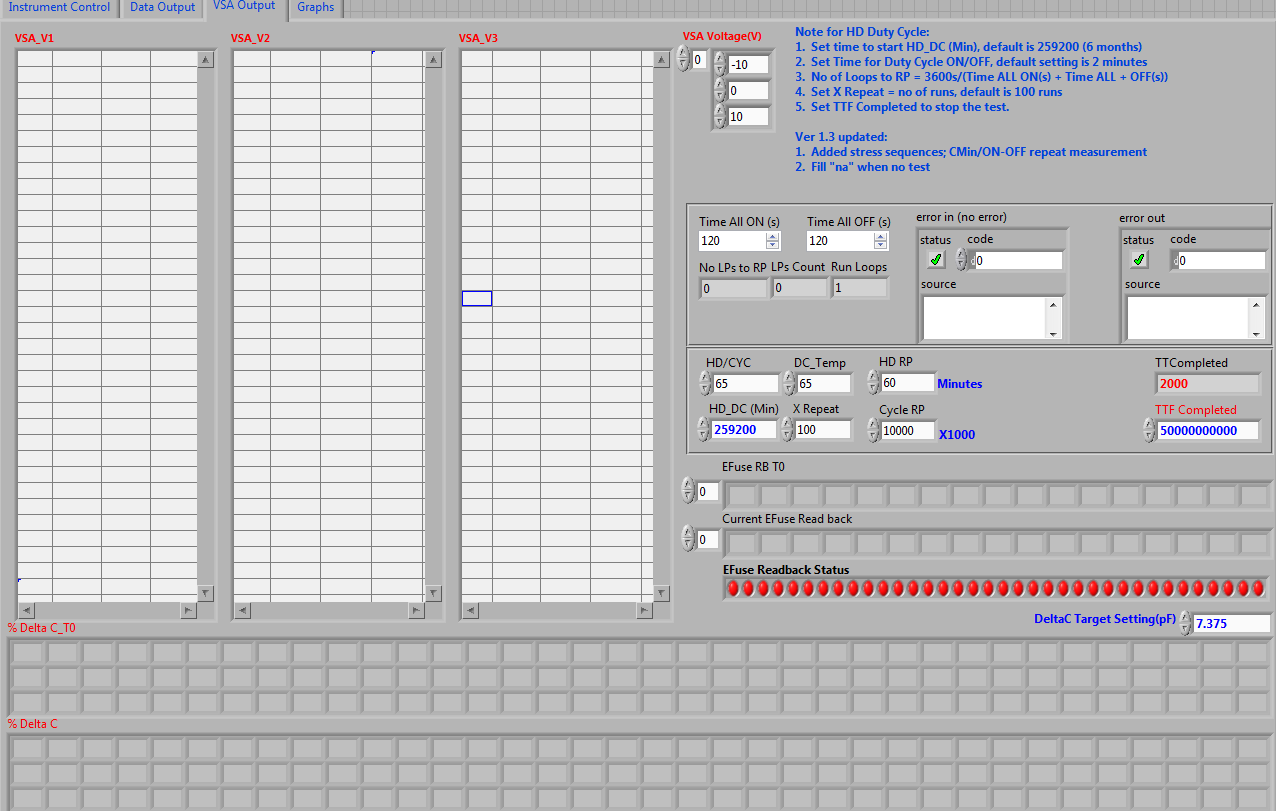
1. Main GUI for calibration and set up test:



1. GUI to monitor the test setup (CP voltage, DVA ON/OFF, ECAL ON/OFF) before stress, monitor cap values for each drivers, and time completed stress



1. GUI to monitor VSA test, HS check, EFUSE read back and % Delta C change



1. GUI to monitor CMIN changes during the stress

